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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,095	08/25/2000	Akella V.S. Satya	KLA1P016F	4627

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/648,095	SATYA ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 07/21/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *108-121* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *108-121* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 108, 109, 114, 115, 116 and 117 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,959,459 to Satya et al. in view of US Patent No. 6,309,956 to Chiang et al.

Regarding claim 108, Satya (figure 1) teaches a method of fabricating a semiconductor die, comprising:

forming a test structure on the semiconductor die (column 3, lines 43-45), wherein the test structure permits voltage contrast testing (column 2, lines 19-23); and

performing voltage contrast testing on the test structure to detect electrical defects within the test structure (column 3, lines 32-42; column 4, line 8 – column 5, line 16).

Satya et al. differ from the claimed invention by not showing a portion of the test structure includes a dummy structure. However, Chiang et al. (figure 5) teach dummy structure (535, 597). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chiang et al. into the method taught by Satya et al. because it improves the strength of semiconductor interlayers, improves mechanical reliability and minimizes dishing between interconnects of semiconductor devices. The combined device shows a portion of the test structure includes a dummy structure.

Regarding claim 109, the combined device shows a substrate (Chiang et al.; 500); and at least one contact (590), which couples the dummy structure (597) to the substrate (500).

Regarding claim 114, the combined device shows forming a plurality of test structures on the semiconductor die, wherein at least a portion of each test structure includes a dummy structure, wherein the test structures permit voltage contrast testing and wherein some of the test structures also include contacts for coupling its dummy structure to a substrate of the semiconductor die and others of the test structures remain floating; and performing voltage contrast testing on the test structures to detect electrical defects within the test structures.

Regarding claim 115, the combined device shows scanning an electron beam over the dummy structures to thereby cause electron emission from the dummy structures; and determining that a particular one of the dummy structures and its associated test structure has a defect between the substrate and the dummy structure by analyzing the electron emission from the dummy structures.

Regarding claim 116, Satya et al. teach the defect is an open defect (column 4, lines 18-23).

Regarding claim 117, the combined device shows a first conductive layer portion (520) underneath the dummy structure (597); and a via (590) coupling the first conductive layer portion (520) to the dummy structure (597).

3. Claims 110, 112, 113, 118 and 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satya et al. in view of Chiang et al., and further in view of US Patent No. 6,001,733 to Huang et al.

The disclosures of Satya et al. and Chiang et al. are discussed as applied to claims 108-109 and 114-117 above.

Regarding claim 110, the combined device shows a first conductive layer portion (520) over the substrate (500) and underneath the dummy structure (597); a second isolation layer (555) between the first conductive layer portion (520) and the dummy structure (597); and a second contact (590) for coupling the first conductive layer portion (520) to the dummy structure (597).

Satya et al. and Chiang et al. differ from the claimed invention by not showing a first isolation layer between the first conductive layer portion and the substrate. However, Huang et al. (figures 3A-E) teach a first isolation layer (304) between the first conductive layer portion (330) and the substrate (300). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Huang et al. into the method taught by Satya et al. and Chiang et al. because it reduces the coupling capacitance between conductive layer and substrate.

Satya et al. and Chiang et al. further differ from the claimed invention by not showing a first contact for coupling the substrate to the first conductive layer portion. However, Huang et al. (figures 3A-E) teach a first contact (via [324]) for coupling the substrate (300) to the first conductive layer portion (330). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Huang et al. into the method taught by Satya et al. and Chiang et al. because it provides interconnection between substrate and conductive layer.

The combined device shows a first isolation layer between the first conductive layer portion and the substrate, and a first contact for coupling the substrate to the first conductive layer portion.

Regarding claim 112, the combined device shows scanning an electron beam over the dummy structure to thereby cause electron emission from the dummy structure; and determining that the test structure has a defect between the substrate and the dummy structure when electron emission is impeded from the dummy structure.

Regarding claim 113, Satya et al. teach the defect is an open defect (column 4, lines 18-23).

Regarding claim 118, the combined device shows a substrate (500) underneath the first conductive layer portion (520).

Satya et al. and Chiang et al. differ from the claimed invention by not showing a via coupling the first conductive layer portion to the substrate. However, Huang et al. (figures 3A-E) teach a first contact (via [324]) for coupling the substrate (300) to the first conductive layer portion (330). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Huang et al. into the method taught by Satya et al. and Chiang et al. because it provides interconnection between substrate and conductive layer. The combined device shows a via coupling the first conductive layer portion to the substrate.

Regarding claim 120, the combined device shows the test structure comprises a plurality of stacked conductive layers and vias to form a multilevel test structure.

4. Claims 111, 119 and 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satya et al. and Chiang et al. in view of Huang et al., and further in view of US Patent No. 3,861,023 to Bennett.

The disclosures of Satya et al., Chiang et al. and Huang et al. are discussed as applied to claims 110, 112, 113, 118 and 120 above.

Regarding claim 111, Satya et al., Chiang et al. and Huang et al. differ from the claimed invention by not showing at least one of the first and second contacts is a redundant type contact. However, Bennett teaches redundant via (column 15, lines 32-42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Bennett into the method taught by Satya et al., Chiang et al. and Huang et al. because it provides interconnection between multi-layers. The combined device shows at least one of the first and second contacts is a redundant type contact.

Regarding claim 119, Satya et al., Chiang et al. and Huang et al. differ from the claimed invention by not showing the via is a redundant via. However, Bennett teaches redundant via (column 15, lines 32-42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Bennett into the method taught by Satya et al., Chiang et al. and Huang et al. because it provides interconnection between multi-layers.

Regarding claim 121, Satya et al., Chiang et al. and Huang et al. differ from the claimed invention by not showing the via is a redundant via. However, Bennett teaches redundant via (column 15, lines 32-42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Bennett into the method

taught by Satya et al., Chiang et al. and Huang et al. because it provides interconnection between multi-layers.

Response to Arguments

Applicant's arguments with respect to claims 108-121 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
October 9, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800